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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/769,534	01/26/2001	Hideo Akiyoshi	108397-00025	4906
7590	11/04/2003		EXAMINER	
AREN'T FOX KINTNER PLOTKIN & KAHN, PLLC Suite 600 1050 Connecticut Ave, N.W. Washington, DC 20036-5339			ENGLUND, TERRY LEE	
			ART UNIT	PAPER NUMBER
				2816

DATE MAILED: 11/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/769,534	AKIYOSHI, HIDEO
	Examiner Terry L Englund	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 21 August 2003.

2a) This action is **FINAL**.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1,2,4-12,14-18 and 20 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) 4 and 14 is/are allowed.

6) Claim(s) 1,2,5,7-12,15-18 and 20 is/are rejected.

7) Claim(s) 6 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 22 August 2002 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.

4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to RCE/Amendment***

The RCE and amendment submitted on Aug 21, 2003 were reviewed and considered with the following results:

Both the RCE and amendment have been entered.

The comments with respect to claims 18 and 20 on page 10 of the amendment overcame the rejections of claims 18 and 20 under 35 U.S.C. 112. It is now understood that the “having pulses” of claim 18 relates to the specific rectangular pulse sections of PLSH, PSL, and POR shown under “(2) :typ.” in the applicants’ Fig. 3. For example, the main power-on reset signal POR shown in “(h)” has two rectangular pulses. The left rectangular pulse corresponds to sub power-on reset signal PLSH’s rectangular pulse, and the right rectangular pulse corresponds to sub power-on reset signal PSL’s rectangular pulse. Therefore, it is understood what “said power-on reset signal having pulses respectively corresponding to each of said sub power-on reset signals” means in claim 18. Also, the rectangular sections of PLSH and PSL power-on reset signals are never shown overlapping each other. Therefore, the “having pulses not overlapping each other” within claim 20 is now better understood. Due to the above understanding of the claimed limitations with respect to the applicants’ Fig. 3, the rejections of claims 18 and 20 under 35 U.S.C. 112 have been withdrawn. However, some of the amended claim changes created new concerns, which are described later under the appropriate section.

The cancellation of claims 3, 13, and 19 rendered their respective rejections moot.

Although the amended claims and comments overcame the rejections of claims 2 and 10 under 35 U.S.C. 102(e) with respect to Zhou et al.; claim 1 under 35 U.S.C. 102(e) with respect

Art Unit: 2816

to Lee; claims 11 and 20 under 35 U.S.C. 103(a) with respect to Zhou et al.; claims 8, 9, and 18 under 35 U.S.C. 103(a) also with respect to Lee; claim 15 under 35 U.S.C. 103(a) with respect to Malherbe/Lee; and claim 15 under 35 U.S.C. 103(a) with respect to Crotty/Lee, they did not overcome the rejections of claims 1, and 7 under 35 U.S.C. 102(e) with respect to Zhou et al.; claims 8, 9, 11, 18, and 20 under 35 U.S.C. 103(a) with respect to Zhou et al.; and claims 5, and 15 under 35 U.S.C. 103(a) with respect to Zhou et al./Lee. The Zhou reference does not clearly show or disclose the plurality of pulse generators as now understood with respect to the recited limitations within claims 2 and 10, or the generation of both a plurality of sub power-on reset signals and pulse signals as recited within claim 11. The Lee reference shows reset signal (N46) actually depends on reset signal N45 instead of the signals being independent of each other as now recited within the claims. Although each of Malherbe's and Crotty's circuits has independently generated reset signals, neither of the references clearly shows or discloses the main reset signal generator's pulse signal having at least one rectangular pulse (understood to have a pair of corresponding leading and lagging edges) as now recited within claim 15. Therefore, the prior art rejections of those claims that have been overcome have been withdrawn, while the other claim rejections have been modified to take into account the amended changes. These modified rejections are described later under the appropriate section, and comments related to the applicant's amended changes and comments are described later under the Response to Arguments section.

It is also noted that the allowability of claims 12 and 17, cited on page 12 of the previous Office Action, has now been withdrawn. After reconsidering the claimed limitations, and various Prior Art references, it was determined at least one reference can be interpreted as

Art Unit: 2816

reading on the claimed limitations. Therefore, these rejections are described later under the appropriate section.

***Claim Objections***

Claims 11 and 14 are objected to because of the following informalities: Claim 11, line 4 should have --each-- added prior to “according” since that was cited in the previous version of the claim, and the presently amended claim does not show any indication that term was meant to have been deleted. For consistent labeling, and to minimize possible confusion, it is suggested --generators-- be added after the first occurrence of “pulse” on line 10 of claim 14. Also, it is noted that the previous version of claim 14 cited “pulse generators”, wherein the presently amended claim does not provide any indication that the term “generators” was meant to be deleted. Appropriate corrections are required.

***Claim Rejections under 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 5-11, 15, 16, 18, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not understood what the applicant actually intends to mean by the “independently of each other” limitations now recited within each of independent claims 1, 5, 7, 8, 10, 11, 15, 18, and 20. Unless one sub power-on reset signal is actually based on, or caused by, another one of the sub power-on reset signals, the generation of these signals can be deemed to be independent of one another. However, if they share at least one common signal (e.g. input), does the applicant still consider them independent of each other?

Art Unit: 2816

For example, one of ordinary skill in the art would know that even the applicant's own signals PORH and PORL (e.g. see Fig. 1) are based on what could be considered a common signal (i.e. VCC as it ramps up). Therefore, even though neither signal PORH nor PORL depends on the other, can they actually be considered completely independent of each other since they share that one common signal? It is not clear in claim 7 which signals are actually being considered independent with respect to one another. For example, if the power-on reset signals are generated according to the sub power-on reset signals, how can they be independent with each other? Also, are the sub power-on reset signals independent from one another, or are the generated power-on reset signals independent from one another? Similar to reasoning previously described, it is not understood what the applicant actually intends to mean by the "independently of the first sub reset signal generator" limitation recited within claim 9.

Dependent claims carry over any rejection(s) from any claim upon which they depend. For example, claims 2, 6, and 16 carry over the rejection of claims 1, 5, and 15, respectively.

#### ***Claim Rejections under 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

In so far as being understood, claims 1, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhou et al. (Zhou - 669), a reference cited in the previous Office Action.

Fig. 5 shows what can be deemed a plurality of sub reset signal generators 520,530 for generating a plurality of sub power-on reset signals (at NODE C and NODE D) having different timings (see Figs. 6(D) and 6(E), respectively); and a main reset signal generator 540,550 for generating a pulse signal POR including at least one rectangular pulse (see the pulse between T11 and T14 in Fig. 6(F)) as the main power-on reset signal POR to initialize an internal circuit (e.g. see 110 of Fig. 1). Since neither NODE C nor NODE D depends on one another, they are considered as being generated independently of each other. Also, signal POR is according to at least one from any of the sub power-on reset signals, thus anticipating claim 1. Also, by interpreting the figures differently, power-on reset pulse signals NODE C and NODE D are generated according to a plurality of sub power-on reset signals NODE B and POR1 having different timings from each other; and it is understood signal POR is used to initialize an internal circuit (e.g. 110 of Fig. 1) according to at least one from any of the signals NODE C and NODE D. As shown in Fig. 6, both NODE C and NODE D have at least one rectangular pulse. Since signals NODE C and NODE D are considered to be generated independently of each, claim 7 is anticipated.

In so far as being understood, claims 1, 2, 7-12, 17, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikehashi et al. (Ikehashi), a reference found during a recent update search. Fig. 3 shows a circuit comprising what can be considered a plurality of sub reset signal generators 3/1 for generating a plurality of sub power-on reset signals VN2'/VN2 at different timings from each other (e.g. see Fig. 4), and independently of each other; and a main reset signal generator 4-6 for generating pulse signal Vpwon as a main power-on reset signal, including at least one rectangular pulse (e.g. see the rising and falling edges of pulse signal

V<sub>pwon</sub> shown in Fig. 4) according to at least one from any of sub-power-on reset signals V<sub>N2'</sub>/V<sub>N2</sub>. One of ordinary skill in the art would understand that main power-on reset signal pulse signal V<sub>pwon</sub> is used to initialize an internal circuit once the main power supply voltage V has reached a minimum predetermined level, thus anticipating claim 1. Main reset signal generator 4-6 comprises a plurality of pulse generators 4/5 for respectively generating pulses V<sub>N3'</sub>/V<sub>N3</sub> on the basis of a transition edge of a corresponding one of the sub power-on reset signals V<sub>N2'</sub>/V<sub>N2</sub> (e.g. V<sub>N3'</sub> corresponds to the leading edge of V<sub>N2'</sub>, and V<sub>N3</sub> corresponds to the trailing edge of V<sub>N2</sub> as shown in Fig. 4); and a composite circuit 6 for synthesizing the pulses to generate main power-on reset signal V<sub>pwon</sub>, anticipating claim 2. Interpreting the circuit of Fig. 3, and the waveforms of Fig. 4, to correspond to a method for initializing a circuit (understood to be receiving signal V<sub>pwon</sub>), pulse signals V<sub>N3'</sub>/V<sub>N3</sub> are generated as power-on reset signals according to sub power-on reset signals V<sub>N2'</sub>/V<sub>N2</sub> at different timings, and V<sub>pwon</sub> is used to initialize the subsequent circuit (not shown, but understood) according to at least one from any of the power-on reset signals. Since power-on reset signals V<sub>N3'</sub>/V<sub>N3</sub> are each shown with a rectangular pulse in Fig. 4, claim 7 is anticipated. First sub reset signal generator 3 includes first transistor M<sub>2'</sub>, and when its threshold value (e.g. corresponding to V<sub>2</sub>) is reached, first transistor M<sub>2'</sub> allows first sub power-on reset signal V<sub>N2'</sub> to go high. Similarly, second sub reset signal generator 1 includes second transistor M<sub>2</sub>, and when its threshold value (e.g. corresponding to V<sub>1</sub>) is reached, second transistor M<sub>2</sub> allows second sub power-on reset signal V<sub>N2</sub> to go high. Combining this understanding with the same reasoning as previously applied to claims 1 and 7, claims 8 and 9 are also anticipated. The limitations of claim 10 closely correspond to claim 2. Therefore, it is understood that the plurality of sub reset signal generators

3/1 generate a plurality of sub power-on reset signals VN2'/VN2 at timings different and independent from each other; a plurality of pulse generators 4/5 generate pulses VN3'/VN3 based on signals VN2'/VN2 with at least one of the pulses having a rectangular pulse; and composite circuit 6 for synthesizing pulses VN3'/VN3 to generate main power-on reset signal Vpwon, anticipating claim 10. Since sub power-on reset signals VN2'/VN2 are generated according to the respective threshold values of transistors M2'/M2, power-on reset signals VN3'/VN3 are generated according to signals VN2'/VN2, and Vpwon will be applied to a subsequent internal circuit (not shown but understood) to initialize it, claim 11 is anticipated. Deeming 3,1 as a sub reset signal generator for generating a plurality of sub power-on reset signals VN2'/VN2 with different timings, and 4-6 as a main reset signal generator for generating pulse signal Vpwon as a main power-on reset signal to initialize an internal circuit (not shown), claim 12 is anticipated because main reset signal generator 4-5 includes a plurality of pulse generators 4/5 and composite circuit 6. Generators 4/5 generate pulses VN3'/VN3 having pulses shorter than an interval between transition edges of sub power-on signals VN2'/VN2 (e.g. see Fig. 4). This anticipates claim 12. Since the generated pulse signals VN3'/VN3 are shorter than the interval between transition edges of sub power-on reset signals VN2'/VN2, claim 17 is also anticipated. Again interpreting Ikehashi's invention in a slightly different manner, plurality of sub reset signal generators 3/1 generate a plurality of sub power-on reset signals VN2'/VN2 according to respective threshold values of transistors M2'/M2 and independently of each other; 4/5 generate a plurality of pulse signals VN3'/VN3 as power-on reset signals with pulses that do not overlap (e.g. see Fig. 4), and Vpwon will initialize an internal circuit (not shown) according to at least one of pulses VN3'/VN3. Since Ikehashi does not clearly disclose that the threshold

values of the MOS transistors M2' and M2 are of any special value, they are considered to have typical thresholds. Therefore, claim 20 is anticipated.

***Claim Rejections under 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

In so far as being understood, claims 8, 9, 11, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. (Zhou - 669). Zhou's Fig. 5 shows a circuit comprising a plurality of sub reset signal generators 520 and 530 for generating a plurality of sub power-on reset signals NODE C and NODE D independently of one another (e.g. NODE C does not depend on NODE D, and vice versa); and main reset signal generator 540,550 generates a pulse signal POR including at least one rectangular pulse (see Fig. 6(F)) according to at least one of said signals NODE C and NODE D. However, the reference does not clearly show or disclose the generation of signals NODE C and NODE D on the basis of respective threshold values of transistors. Since section 120 comprises CMOS transistors, it would have been obvious to one of ordinary skill in the art to form each of the inverters (e.g. 522, 527, 532, 534, and 550) as a CMOS inverter, and each of the logic devices (e.g. 524, 528, and 540) could be formed using appropriate combinations of MOS transistors. Each transistor would have its own respective threshold voltage, and it would be understood the inverters and logic devices would trigger when their threshold voltage would be reached. For example, when the respective transistor threshold(s) within path 522,524,527,528 is reached, the appropriate signal NODE C is

generated. Therefore, claim 8 is rendered obvious. The delays and logic devices can be formed from appropriate MOS structures, and their threshold values (e.g. triggering levels) would provide the basis of the signals generated. The MOS transistors would correspond to the MOS transistors shown within section 120 (thus having similar operational characteristics with respect to voltage and temperature); would be easier to fabricate on an IC; and consume less power than bipolar transistors. For similar reasons, first sub reset signal generator 520 will generate first sub power-on reset signal NODE C on the basis of a first threshold value of a first transistor within generator 520 (e.g. a transistor within inverter 522); second sub reset signal generator 530 will generate second sub power-on reset signal NODE D on the basis of a second threshold value of a second transistor within generator 530 (e.g. a transistor within inverter 532); and main reset signal generator 540,550 will generate pulse signal POR (having a rectangular pulse as shown in Fig. 6(F)) to initialize an internal circuit (e.g. 110 of Fig. 1), rendering claim 9 obvious. Using transistors in each of the inverter's within Zhou's Fig. 5, signal POR has what can be deemed two pulses (i.e. one main low to high transition pulse, and one rectangular pulse between T11 and T14), wherein signal POR corresponds to the sub power-on reset signals (e.g. POR1 and NODE B; or NODE C and NODE D). Since there is no reason to use special transistors, it would be obvious to use normal transistors within the inverters. These transistors would have typical values, thus claim 18 is rendered obvious.

In so far as being understood, claims 5, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. (Zhou) in view of Lee's U.S. Patent 5,394,104 ('104) cited in the previous Office Action. As previously described with respect to rejections of closely related claims 1, 7, and 10, Zhou's Fig. 5 shows a circuit comprising what can be deemed a sub reset

signal generator 520,530 for generating sub power-on reset signals NODE C, NODE D; and a main reset signal generator 540,550 for generating pulse signal POR, including at least one rectangular pulse as a main power-on reset signal (see section T11-T14 of Fig. 6 (F)), to initialize an internal circuit (e.g. 110 of Fig. 1) according to the signals received by generator 540,550. However, the reference does not show or disclose the circuit receiving an external power-on reset signal. Lee ('104) shows and discloses the use of an external power-on reset signal (e.g. see 180 in Figs. 1-3B, and 680 in Fig. 6) as an override reset signal (e.g. see column 1, lines 34-35). Therefore, it would have been obvious to one of ordinary skill in the art to also include an external reset signal to Zhou's generator 540,550, rendering claim 5 obvious. The external reset signal would provide a means to reset the circuit, if a need arises, without having to completely power down and then re-apply the power to the system/circuit. [For example, a personal computer typically has a manual reset button to restart/reboot if a computer error occurs (e.g. operation hangs up).] A reset terminal of the integrated circuit would receive the external reset signal, to ensure generator 540,550 would have the capability of receiving the external reset signal supplied from the exterior of the IC, thus rendering claim 15 obvious. The external reset would allow the system/circuit to be reset without the need to turn power completely off.

***Allowable Subject Matter***

Claims 4, and 14 are allowed. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the main reset signal generator includes a plurality of pulse generators for generating pulse corresponding to the sub power-on reset signal(s), and the external power-on reset signal, as recited within independent claims 4, and 14.

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. It depends on claim 5, but has the plurality of pulse generators similar to claims 4 and 14 above.

Claim 16 would also be allowable for the same reasoning as applied to claims 4, 6, and 4 above if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action. Claim 16 depends on rejected claim 15.

*Prior Art*

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed inventions. Although not cited in any formal rejections described above, these references are believed to read on at least some of the basic independent claims. Fig. 2 of Dalrymple shows a plurality of reset signal generators 47,49 generating a plurality of reset signals V4,V5 with different timings (e.g. see Figs. 3B-3C) and independent of one another, wherein these signals are received by a main reset signal generator 63 which provides a main power-on reset type signal V6 with at least one rectangular pulse (e.g. see Fig. 3D). Figs. 2A-2C of Zhou each show a circuit comprising two reset signal generators POR A, POR B, and what can be considered a main reset signal generator (e.g. 206,208 of Fig. 2A, , 508,510 of Fig. 2B, and 708,710 of Fig. 2C. The reset signals of POR A and POR B each show rectangular pulses (e.g. see Fig. 4), and the main output reset signal POR Output can be considered a pulse with a rectangular pulse (having a set of rising and falling edges). Therefore, these references should be carefully reviewed and considered.

***Response to Arguments***

The applicant's argument with respect to independent signals does not comply with 37 CFR 1.111(c) because it does not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. Although the signals N46 and N45 of Lee are clearly not independent of one another, it is not understood why the applicant does not consider Zhou's signals NODE C and NODE D independent of one another. For example, even though both those signals depend on common signal POR1, signal NODE C does not depend on NODE D, and vice versa. Therefore, that reference's signals can still be deemed independent of one another.

Therefore, the rejections cited in the previous, and the present Office Action, are deemed proper with respect to how the claimed limitations can be interpreted.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

  
Terry L. Englund  
3 November 2003



TIMOTHY P. CALLAHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800